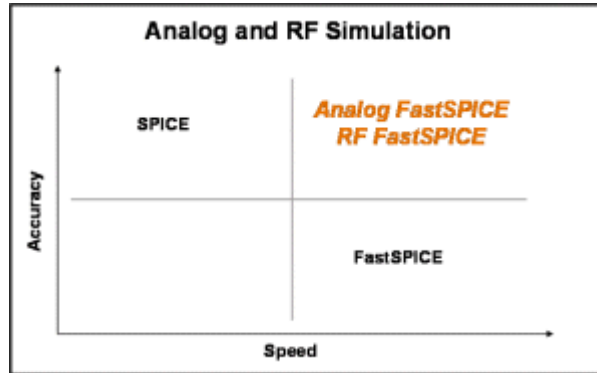


PLL Noise Analyzer™



True-SPICE Accuracy, 5X-10X Faster, No Tuning for Analog/RF Designs

Overview

PLL Noise Analyzer™ is the industry's first noise analysis tool for phase-locked loops (PLLs). *PLL Noise Analyzer* addresses a leading cause of silicon re-spins - analog noise and jitter - enabling circuit designers to reliably meet cost, performance, and schedule goals. *PLL Noise Analyzer* is based on Berkeley Design Automation's proprietary *Precision Circuit Analysis™* technology which delivers fast and accurate circuit analysis results. It includes the company's Stochastic Nonlinear Engine™, which provides fast and accurate analysis of the nonlinear, time-varying behavior of full PLL circuits at the transistor-level. *PLL Noise Analyzer* provides complete phase noise and jitter analysis for noise caused by all sources - random and deterministic - that are inherent or external to the PLL. The tool also provides a complete view of the noise contributors as well as the circuit node sensitivity to noise injection. *PLL Noise Analyzer* eliminates the need for manual, error-prone model generation and the inaccurate, linear approximations traditionally used for PLL noise analysis.

Key Features

- Fast and accurate phase noise and jitter analysis of full PLLs (integer-N)
- Quick identification of top circuit noise contributors
- Thorough analysis of circuit noise sensitivity
- Easy integration with existing analog verification flows

Target Applications

- Integer N, non-differential PLLs used in clocking, wireless, graphics, high speed I/O, networking, and processor applications

Technology

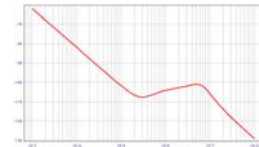
The foundation of *PLL Noise Analyzer* is the Stochastic Nonlinear Engine. The Stochastic Nonlinear Engine is a set of proprietary algorithms that quickly and efficiently solve the stochastic nonlinear partial differential equations that accurately model the nonlinear, time-varying behavior of circuits such as PLLs at the transistor level. Berkeley Design Automation pioneered this technology which combines time and frequency domain analyses engines. The Stochastic Nonlinear Engine has been proven to deliver accurate noise and jitter analysis results on a wide variety of designs spanning geometries from 0.35 μm to 65nm.



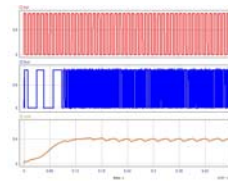
Full PLL Noise Analysis

PLL Noise Analyzer performs the following analyses for PLLs:

- Random noise analysis
- Deterministic noise analysis
- Locking behavior verification



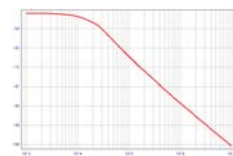
Users can perform phase noise and jitter analysis on the full, transistor-level netlist. This analysis calculates the random noise caused by the circuit itself (inherent) and by external sources. The user can selectively view the noise results block-by-block to diagnose which blocks contribute the most noise. Results are shown in terms of both phase noise and jitter.



Designers can also run deterministic noise and jitter analysis which calculates noise due to inherent and external sources such as supply voltage ripple and clocking noise injection from the switching of digital circuits. This analysis produces the minimum, maximum and average PLL clock period as well as eye diagrams.

Block-Level Noise Analysis

The periodic behavior and noise performance of all blocks in a PLL can be verified with *PLL Noise Analyzer*. Designers can quickly perform periodic noise and jitter and periodic steady-state (PSS) analysis on a block-by-block basis on the reference block, dividers (reference divider, feedback dividers), phase detector, charge pump, loop filter, and voltage controlled oscillator (VCO).



PLL Noise Analyzer provides noise results in both frequency domain (as phase noise spectra) and time domain (as jitter). It lists the top noise contributors along with their percent noise contribution, allowing the designer to focus on the most critical devices in order to optimize the design.

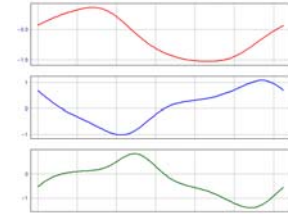


Periodic steady-state analysis allows designers to verify the operation of each block with periodic outputs – frequency dividers, VCO, and phase detector. For the phase detector, *PLL Noise*

Analyzer automatically runs a separate PSS analysis for the lead, lag, and in-phase cases of the up and down inputs.

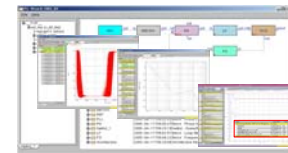
Powerful Noise Sensitivity Analysis

The Stochastic Nonlinear Engine has the ability to list the top noise contributors – noise sources based on their percent noise contribution – and to combine the circuit's sensitivity to each noise source with the noise source intensity. This gives the designer the powerful ability to reduce noise by either reducing the noise source intensity through device optimizations and/or modifying the circuit's sensitivity to the noise source through circuit optimizations. The user can incrementally update the design after optimization and quickly re-analyze noise.

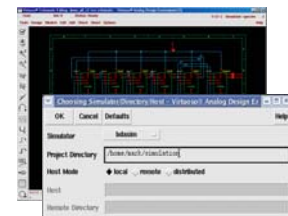


Fits Your Existing Flow

PLL Noise Analyzer easily fits into existing HSPICE and Spectre-based verification flows. It reads standard HSPICE and Spectre-format netlists and supports popular device model formats, including BSIM3, BSIM4, Gummel-Poon, MOS11, and Mextram.



A graphical user interface (GUI) guides the user through the entire PLL analysis process, from design setup to analysis and viewing results, and automates the creation of a noise analysis test bench. Integration into Cadence's Analog Design Environment allows designers to easily invoke *PLL Noise Analyzer* from within ADE. Results can be viewed with BDA's waveform viewer, WaveCrave, or third party waveform viewers from Sandwork, Cadence, and Synopsys.



Feature Summary

- Analyses: Phase noise and jitter analysis of integer-N PLLs
- Netlist: HSPICE and Spectre formats
- Models: BSIM3, BSIM4, Verilog-A, Gummel-Poon, MOS11, Mextram, s-parameter
- Outputs: PSF ASCII, PSF binary, Nutmeg ASCII, Nutbin, Nutbinf
- Integrated into the Cadence Virtuoso Analog Design Environment (ADE)
- Advanced waveform viewing with BDA's WaveCrave viewer

Platform Support

PLL Noise Analyzer is available for SUN and Linux operating systems.

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