

**Efficient Noise Analysis
for Complex Non-Periodic Analog/RF Blocks**

Berkeley Design Automation, Inc.

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1 Introduction

Noise minimization is a required design objective for advanced analog and RF circuits. Unlike digital circuits, where noise is a second-order effect, noise in analog and RF circuits directly affects system performance metrics such as signal to noise ratio (SNR) and bit error rate (BER). Effective design optimization in the presence of random device noise is challenging because the noise sources are inherent in the circuit elements and cannot be eliminated. Because device noise determines the fundamental limits on circuit performance, it plays a significant role in analog/RF circuit design. [1]

Noise-related issues become particularly critical in circuits that have noise-sensitive architectures, have tight specifications, and are implemented in bulk CMOS processes with low voltage levels and high frequencies. Most common complex blocks, including ADCs, PLLs, transmit chains, receive chains, high-speed I/Os, and DC:DC converters, are highly susceptible to noise.

Traditional SPICE and RF tools cannot handle noise analysis of today's complex circuits due to convergence, accuracy, and performance limitations. Very few design teams perform transistor-level noise analysis at the complex-block level, and many designers must simplify even more complex subcircuits (such as VCOs with buffer, bias, and divider) to perform noise analysis. Digital fastSPICE tools do not offer noise analysis capabilities, and given their high levels of inaccuracy, using digital fastSPICE tools for transient noise analysis would be meaningless.

Berkeley Design Automation provides comprehensive, world-class noise analysis with characteristics that parallel those for its transient simulation: true SPICE accuracy, 5x-10x higher performance, and 5x-10x higher effective capacity. These capabilities make it practical, for the first time, to thoroughly characterize noise in sensitive complex blocks including sigma-delta ADCs, fractional-N PLLs, SerDes/CDRs, and DC:DC converters.

This white paper provides an overview of noise in semiconductors and noise analysis methods. It continues with a detailed description of transient noise analysis, its application to non-periodic complex blocks, and its implementation in the Berkeley Design Automation Noise Analysis Option (NAO) for the company's Analog FastSPICE™ (AFS) circuit simulator. This paper concludes with NAO transient noise analysis results for a number of challenging production circuits.

2 Noise in Gigahertz Nanometer Circuits

Noise fundamentally limits integrated circuit performance. There are two major noise categories: random and deterministic. Random noise is inherent in semiconductor device physics. Deterministic noise, on the other hand, has specific non-inherent sources.

Random Noise

Random noise is defined as unpredictable electronic noise. Random noise typically follows a Gaussian distribution, also referred to as normal distribution. In addition, the composite effect of many uncorrelated random noise sources, regardless of their distributions, approaches a Gaussian distribution. White noise and flicker noise are the two dominant random noise sources in semiconductor devices. [1]

White Noise

White noise is a random signal with a flat spectral density. The primary sources of white noise are thermal noise and shot noise. In analog/RF CMOS circuits the main white noise source is MOS device channel thermal noise.

Thermal noise results from voltage fluctuations caused by the Brownian motion of electrons in a resistive medium. Thermal noise is found in both passive and active devices. It is broadband white noise that intensifies as temperature increases. Thermal noise has a Gaussian amplitude distribution in the time domain and its power is evenly distributed across the frequency spectrum. Thermal noise dominates in many applications.

Shot noise derives from the discrete quantum nature of electron flow through a potential barrier. It is most often associated with diodes and bipolar transistors. Shot noise is due to the fact that current flowing across a junction is not smooth, but is comprised of individual electrons arriving at the junction at random times. This non-uniform flow creates broadband white noise that increases with increasing average current.

Flicker Noise

Flicker noise, also referred to as $1/f$ noise, is due to traps in semiconductors where carriers that would normally constitute DC current flow are captured for some time and then released. Flicker noise process correlation times are very long, which makes the power spectral density of flicker noise proportional to $1/f$. The frequency at which the flicker noise spectral density approximates the flat white noise spectral density is referred to as the $1/f$ corner frequency. Flicker noise exists in all active devices. It is a significant noise source in MOS devices, but not in bipolar devices.

Flicker noise in the drain current of a MOS device is important for analog and RF circuits. At low frequencies flicker noise is the dominant noise source in MOS devices. Noise in MOS devices typically has a spectrum with a slope ~ -0.7 and ~ -1.3 in a log-log plot. MOS device flicker noise can also have a serious impact on RF CMOS circuits at high frequencies when there is noise upconversion.

Figure 1 illustrates the spectral density for thermal and flicker noise, with flicker noise dominating at low frequencies and a flat spectral density for thermal noise and the upconversion of flicker noise at higher frequencies. [2]

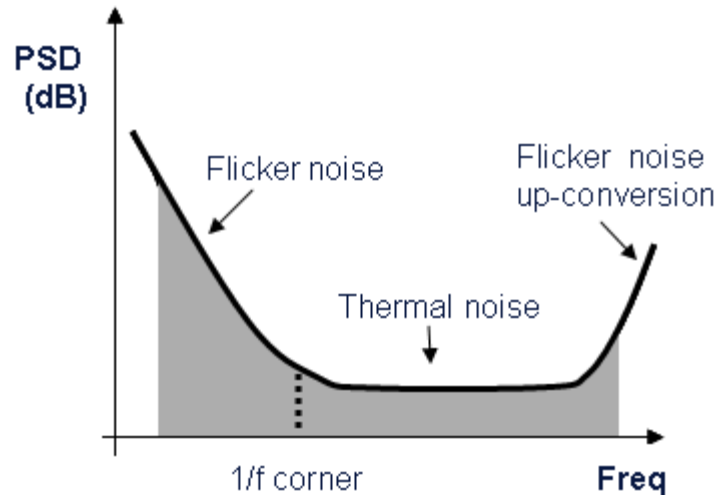


Figure 1. Thermal and Flicker Noise Spectrum

Deterministic Noise

Deterministic noise occurs when undesired signals from other blocks in the system are coupled into sensitive analog/RF nodes through the power supply, substrate, package, and so forth. Deterministic noise has a non-Gaussian distribution, has bounded amplitude, and typically can be traced to a specific cause. The sources of deterministic noise include crosstalk, electromagnetic interference (EMI), power supply noise, and substrate noise.

Crosstalk between adjacent signal traces occurs when electrical activity on one conductor induces current on another. This induced current changes the voltage, thereby causing noise. In the case of EMI radiation, a sensitive signal path is affected by the magnetic field from an EMI source. EMI sources include power supplies, AC power lines, and RF-signal sources. Like crosstalk, EMI induces a noise current on the timing signal path, which modulates the timing signal voltage level to create noise.

Power and ground are other deterministic noise sources. When noise shifts the power or the ground reference, the threshold voltage required to switch a control gate or alter an analog level also changes. On the digital side of a mixed-signal block, when multiple gates switch to the same logic state simultaneously, they can introduce current spikes to the power and ground planes. Those spikes can create threshold voltage-level shifts.

Substrate noise results from unwanted substrate coupling to sensitive circuitry. Both digital circuitry and on-chip oscillators can inject substrate noise. Injected noise propagates along an AC path to ground. Devices and interconnect can pick up this noise from the substrate, and the circuit can lose signal power to the substrate. Modeling substrate noise is difficult both because the model must include the entire die and because

the substrate is only one piece of a larger RLC network that includes the associated interconnect, the package, and related printed circuit board traces.

It is possible to analyze deterministic noise by modeling the noise sources and running a SPICE transient simulation. However, designers often use specialized signal integrity and EMI characterization tools.

The remainder of this paper focuses exclusively on random noise and its analysis.

Circuit Impact of Random Noise

Phase noise is an example of the impact random noise has in analog and RF circuits. Phase noise is the frequency-domain representation of unwanted time-domain noise or jitter. Without phase noise, an ideal oscillator or phase-locked loop (PLL) would generate a pure sine wave and all of the signal power would occur at that frequency. However, real oscillators and PLLs have phase-modulated noise components.

Oscillators produce relatively high levels of noise at frequencies close to the oscillation frequency. Because the noise is near the oscillation frequency, it is not possible to filter the noise without also removing the oscillation signal. Moreover, because this noise is predominantly in phase with the oscillation, it is not possible to remove the noise by passing the signal through a limiter.

Phase noise has a significant impact in communications systems. Figure 2 illustrates the effects of phase noise on a receiver channel. In a receiver, the phase noise of the LO can mix with a large interfering signal from a neighboring channel and overwhelm the signal from the desired channel, even though most of the power in the interfering IF gets removed by the IF filter. This process is referred to as reciprocal mixing. [3]

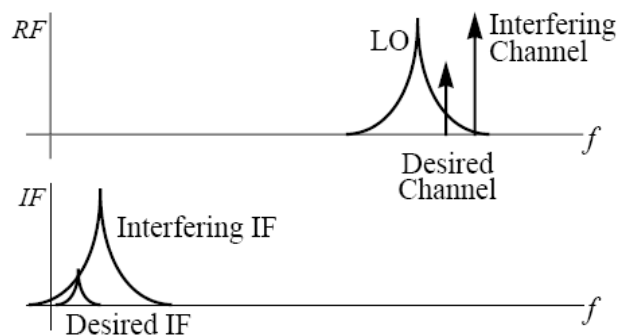


Figure 2. Receiver Interference Example

3 Noise Analysis Methods

This section describes transistor-level noise analysis methods including transient noise analysis, periodic noise analysis, and oscillator noise analysis.

The simulator noise floor is of primary concern in any transient-based noise analysis because it determines the noise resolution. The SPICE noise floor is a function of the simulator integration algorithms and basic SPICE parameters such as `reltol` and `maxstep`. The noise floor with default SPICE settings is typically on the range of 0.1%. Poor SPICE simulator computational methods, inherent simulator inaccuracies (e.g., in digital fastSPICE simulators), or relaxed tolerance settings severely adversely impact the noise floor. For example, 1% simulator inaccuracy can result in reported ADC power spectral density (PSD) that is 20dB higher than that for a simulator with true SPICE accuracy (~0.1%). Such results are dangerously misleading especially considering the actual device noise for the same circuit is only ~10 dB range.

SPICE simulators include small-signal AC analysis that calculates the noise contributed by various devices as a function of frequency. This noise analysis applies to simple circuits only such as amplifiers and filters that operate at a constant DC operating point. Beyond AC noise analysis, there are three main transistor-level noise analysis methods:

Transient Noise Analysis injects random noise for each device noise source at each timestep during transient simulation to produce output waveforms that include realistic noise effects. Post-processing the noisy waveforms translates the noise to the frequency domain. This technique is valid for all circuit types and is the only transistor-level noise analysis technique for non-periodic circuits such as sigma-delta ADCs and frac-N PLLs. Although some traditional SPICE simulators have offered transient noise analysis, the runtimes are so long that the analysis is infeasible for even moderately-complex blocks.

Periodic Noise Analysis (`pnoise`) computes the noise of periodically-driven circuits such as mixers, switched-capacitor filters, phase detectors, charge pumps, and dividers. `Pnoise` analysis is faster than transient noise analysis for these types of circuits and provides additional diagnostic information such as noise source contributions.

Oscillator Noise Analysis (`oscnoise/vconoise`) computes the phase noise of periodic autonomous circuits such as VCOs (LC-tank and ring-oscillator circuits) and crystal oscillators. `oscnoise/vconoise` analysis is faster than transient noise analysis for this type of circuit and, like periodic noise analysis, can provide noise source contributions. Advanced `oscnoise/vconoise` techniques do not make linear approximations that sacrifice accuracy, and also provide impulse sensitivity function (ISF) waveforms for every node, which is very valuable during oscillator phase noise optimization.

Table 1 summarizes which random noise analysis methods are applicable to various types of circuits. Noise analysis for complex blocks such as ADCs and PLLs starts with analyzing each subcircuit using the most appropriate technique. Once the subcircuits are complete, a transient noise analysis of the entire complex block can measure top-level noise performance, including noise effects due to interactions between subcircuits.

Table 1. Random Noise Analysis Applications

Noise Analysis Option Feature	Transient Noise	Pnoise	Oscnoise
Non-Periodic Circuits			
Frac-N PLLs	✓		
Int-N PLLs	✓		
ADCs (sigma-delta, pipelined, etc.)	✓		
Tx chains	✓		
Rx chains	✓		
PHYs	✓		
SerDes	✓		
Periodic Driven Circuits			
Switched cap filters	✓	✓	
Mixers	✓	✓	
Phase detectors	✓	✓	
Charge pumps	✓	✓	
Dividers	✓	✓	
Periodic Autonomous Circuits			
VCOs	✓		✓
Crystal osc (XO)	✓		✓
LC-tank VCOs	✓		✓
Ring VCOs	✓		✓

The remainder of this paper focuses on transient noise analysis and its applications.

4 Transient Noise Analysis

Transient noise analysis simulates the response of a circuit to random device noise (white and/or flicker). Figure 3 illustrates a simplified transistor noise model and the resulting waveforms from a normal transient simulation and the equivalent transient noise analysis.

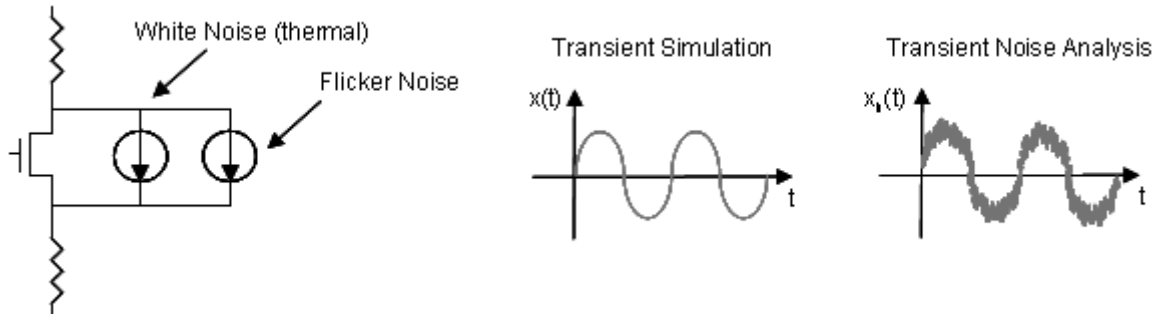


Figure 3. Transient Noise Modeling

Transient noise analysis models transistor noise as current sources with random values based on the noise intensity information from the device model. Because it is statistically-based, the accuracy of transient noise analysis is a function of the number of random samples simulated, i.e., the simulation interval. In addition to the sample size, two key considerations are the device noise models and results post-processing.

Device Noise Models

SPICE device models include parameters for random noise. The results of transient noise analysis depend on the noise model equations and the noise model parameters.

The main theories used for flicker noise in MOS device models are:

- Carrier Number Fluctuation Theory: attributes noise to the capture and release of charge carriers in traps located in the gate dielectric.
- Mobility Fluctuation Theory: attributes noise to bulk mobility fluctuations caused by phonon scattering.
- Unified Noise Model: extends the Carrier Number Fluctuation Theory to include the Coulomb scattering of free charge carriers at trapped oxide charge carriers.

The Unified Noise Model for flicker noise has gained wide acceptance. This model assumes that the carrier numbers in the channel fluctuate due to traps in the gate oxide, and that these fluctuations affect the carrier mobility, which results in (correlated) mobility fluctuations. Most compact MOS device models (BSIM3, BSIM4, MOS Model 9, and MOS Model 11) use the Unified Noise Model. [4]

Thermal noise is the dominant source of noise at RF frequencies, where flicker noise becomes negligible. There are several approaches to modeling drain current thermal noise in MOS devices, including the ones implemented in the MOS11 and BSIM4 models.

The MOS11 channel segmentation model calculates thermal noise with the Klaassen–Prins equation, which includes the effect of channel length modulation. This model assumes that charge carriers are in thermal equilibrium. Therefore, the Nyquist expression yields the voltage noise spectral density of a channel segment and the noise sources of different channel segments are uncorrelated. The effect of velocity saturation in the channel region is included through local channel conductance. As shown in Figure 4, the MOS11 model is based on the concept of channel segmentation. [4]

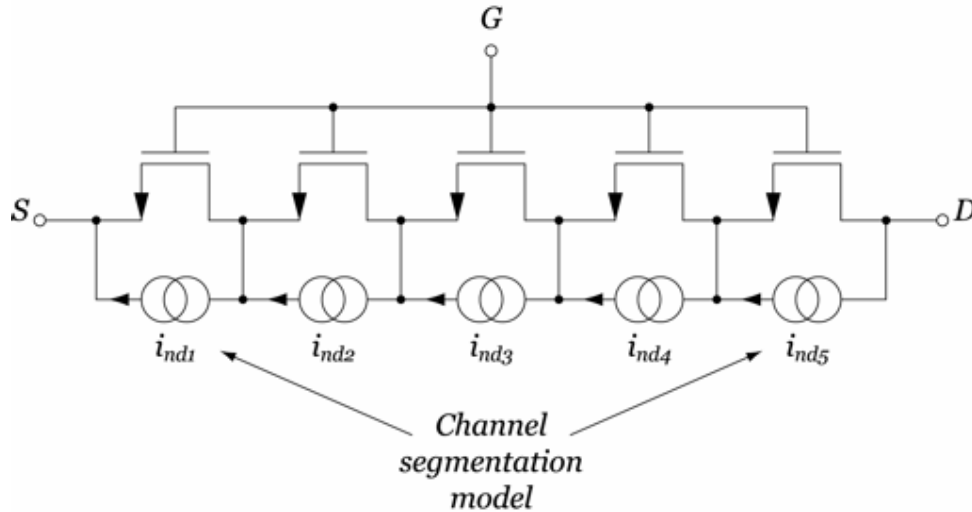


Figure 4. MOS11 Noise Model

There are two channel thermal noise models in BSIM4: charge-based and holistic. The holistic thermal noise model includes all short-channel and velocity saturation effects. In addition, channel thermal noise amplification through G_m and G_{mbs} and induced-gate noise that is partially correlated to the channel thermal noise are all captured using “noise partition.” Figure 5 shows schematically that some of the channel thermal noise source is assigned to the source side. [5]

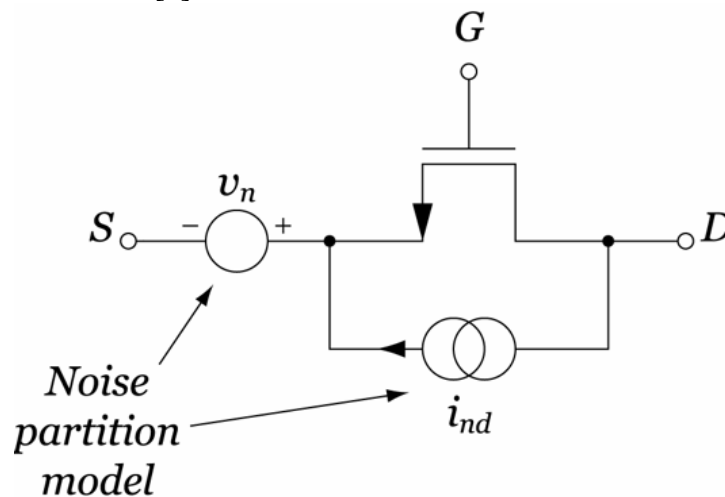


Figure 5. BSIM4 Noise Model

Results Post-Processing

FFT-based post-processing translates transient noise analysis results from the time domain to the frequency domain. It does so by sampling a continuous waveform and computing its power spectral density (PSD). From the power spectral density, one can calculate noise metrics such as:

- Signal-to-Noise Ratio (SNR)
- Signal-to-Noise-plus-Distortion Ratio (SNDR)
- Spurious-Free Dynamic Range (SFDR)
- Total-Harmonic-Distortion (THD)
- Phase noise

Figure 6 illustrates the post-processing methodology for an ADC. The FFT-based post-processing steps are as follows:

1. Sample the waveform at the sampling rate of F_{sample}
2. Divide the data into segments of $nfft$ data points
3. Compute the FFT of each segment
4. Compute the average power

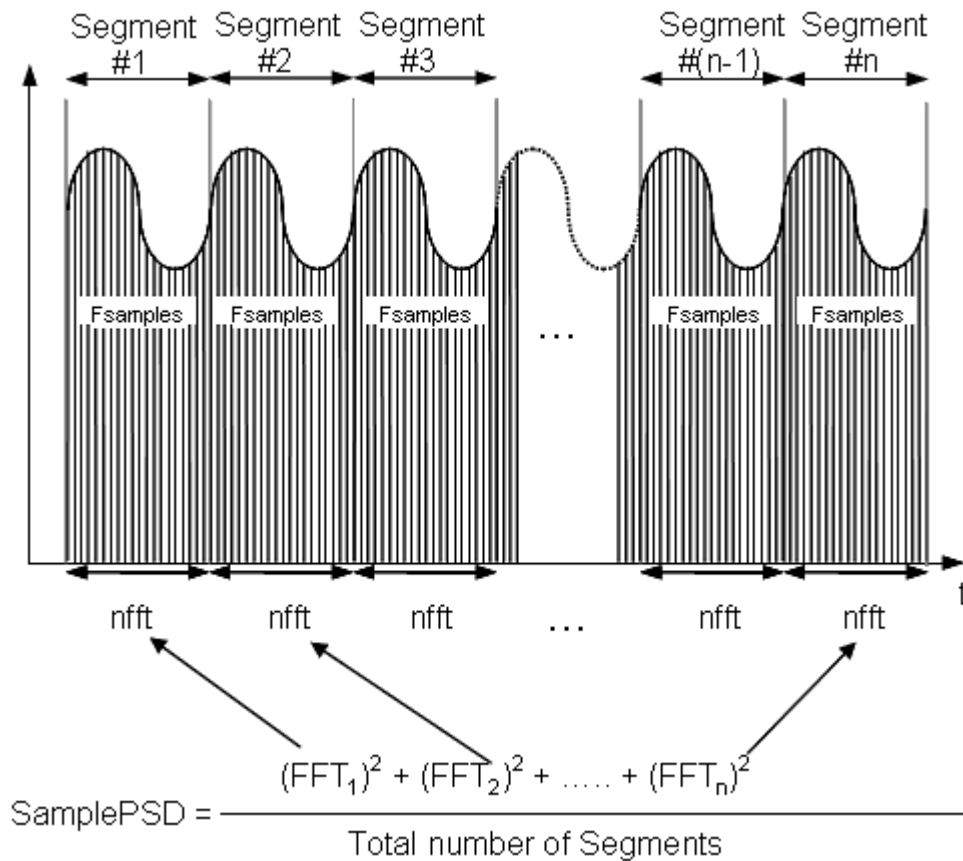


Figure 6. Power Spectral Density Calculation via FFT-Based Post-Processing

Random variation and spectral leakage from one frequency bin to adjacent frequency bins can introduce errors into the power spectral density calculation. The confidence interval for power spectral density is proportional to $1/\sqrt{K}$, where K is the number of data segments used in the power spectral density estimation. [6] Longer simulation intervals and using more data segments tighten the confidence limits.

Figure 7 shows an example of a post-processed spectrum for a sigma-delta ADC. It clearly shows that device noise dramatically reduces circuit performance.

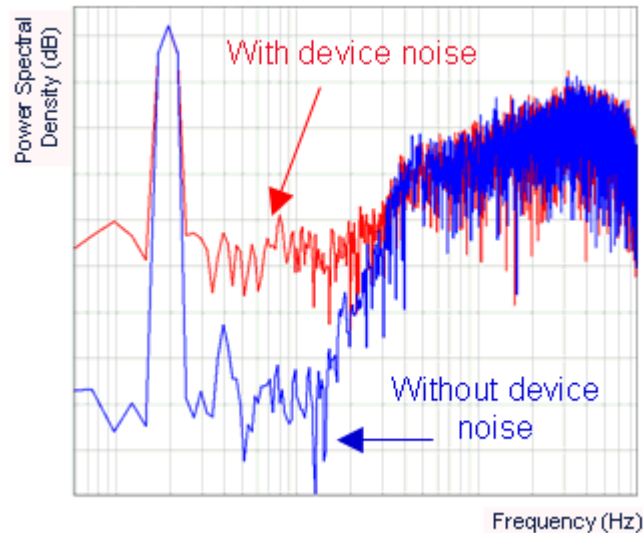


Figure 7. Post-Processing Results for an ADC

5 Transient Noise Analysis Application and Validation

The transient noise analysis use model is a simple extension of regular transient simulation. Designers include additional parameters that specify the desired noise (white and optionally flicker) and can turn off noise for specified subcircuits. Table 2 lists the transient noise analysis parameters.

Table 2. Transient Noise Analysis Parameters

Parameter	Specifies
noisefmax	Required - turns on white noise and defines the bandwidth for noise sources.
noisefmin	Optional - turns on and sets the lower frequency limit for flicker noise sources.
noiseseed	Optional - positive integer value to seed the random number generator.
noisescale	Optional - noise voltage/current scaling factor for all noise sources.

Transient noise analysis applies to any circuit and is very effective for complex blocks. Of particular interest is the application of transient noise analysis to non-periodic complex blocks such as sigma-delta ADCs and frac-N PLLs.

Table 3 shows the recommended analysis parameters for ADC and PLL applications. The key parameters for ADCs are signal frequency (fsignal) and clock frequency (fclock). The key parameters for PLLs are stabilization time (tstab), VCO frequency (fvco), and minimum offset frequency (minfm) in a phase noise measurement.

Table 3. Transient Noise Analysis Parameter Guidelines for ADCs and PLLs

	tstep	tstop	noisefmax	noisefmin
ADC	$1/(20*fclock)$	$tstab + 10/fsignal$	$50 * fclock$	$10/tstop$
PLL	$1/(20*fvco)$	$tstab + 40/minfm$	$50 * fvco$	$10/tstop$

Total simulation time is an important consideration for PLLs if one wants to analyze phase noise at low offset frequencies (for example, to ensure there is no noise folding from a sigma-delta modulator). A good guideline is to run at least 10 cycles of the minimum offset frequency for a basic measurement and to run 40 to 100 cycles to ensure statistically accurate phase noise results. It is possible to dramatically reduce the total runtime by running multiple transient noise simulations in parallel and combining the results in post-processing.

Transient Noise Analysis Validation

There are two reliable ways to validate the results of transient noise analysis: theoretical validation and comparisons (direct or indirect) to measured data.

One simple theoretical validation method is to compare transient noise analysis results with the theoretical value of kT/C noise. When thermal noise is present at a filtering capacitor C , it is referred to as kT/C noise. Consider the simple RC circuit shown in Figure 8, with the output voltage measured across the capacitor. The broadband thermal noise of the resistor is shaped by the low-pass filter. The filter could be a discrete resistor and capacitor pair, or it could be the channel resistance and drain capacitance of a MOS device. The theoretical RMS noise voltage value in a capacitor C is $\sqrt{kT/C}$.

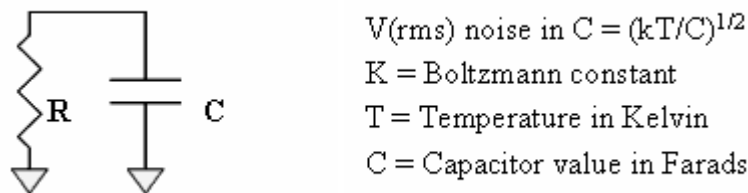


Figure 8. kT/C Noise Experiment

Designers may want to compare transient noise results to the other noise analysis methods such as hand calculations, system simulation estimates, and silicon measurements. In doing so they should be aware of the limitations and challenges in doing so.

A number of factors make it difficult to compare transient noise analysis results between simulators. The simulator noise floor is a critical limitation. As described above, this floor determines the effective noise resolution. Generally, the default SPICE noise floor is within approximately 0.1% of the magnitude of the desired signal. It is often desirable and sometimes even necessary to analyze complex blocks with tighter tolerances to push down the noise floor and increase the noise resolution. Ideally the noise floor should be identical for each method one compares. Another limitation is model accuracy (for example, system-level and device noise models). Accurate comparison requires sufficiently long simulation intervals. Also, subtle post-processing differences can dramatically affect correlation.

Directly comparing transient noise analysis to silicon measurements can be difficult due to differences between the simulation and testbench environments. Test probe loading and setup introduces noise when measuring the desired signal off chip, which reduces the silicon measurement accuracy. Of course, test equipment also has noise floor limitations that limit the resolution.

Another alternative is to indirectly compare transient noise analysis to proven noise analysis methods, such as oscillator noise analysis, that are already correlated to silicon.

6 Analog FastSPICE Transient Simulation

Transient noise analysis is built on transient simulation. Thus it is important to consider the quality of the underlying circuit simulator accuracy and performance. The Berkeley Design Automation Noise Analysis Option is built on the company's Analog FastSPICE (AFS) transient simulation. AFS is proven to deliver true SPICE accuracy with 5x-10x faster performance and 5x-10x higher effective capacity than any other approach.

Accuracy and Performance

Table 4 compares AFS and traditional SPICE runtimes for representative sample of pre-layout and post-layout ADCs and PLLs. Each comparison is with one of the industry's two leading "golden" SPICE simulators with both simulators using the original netlist. In all cases, the circuit designers verified that the AFS waveforms matched "golden" SPICE results down to the SPICE noise floor (generally 0.1% or tighter with reltol = 1E-4 or less). All performance numbers are based on equivalent hardware.

Table 4. AFS Transient Simulation Examples

Circuit	Elements	MOS	SPICE	AFS	Speedup
Pre-Layout					
PLL (3GHz, 130nm)	6K	4K	21 days	20 hrs	22x
PLL (3GHz)	4K	3.8K	78 hrs	5.4 hrs	14x
Sigma-Delta ADC	6K	5K	105 hrs	14 hrs	7x
Pipeline ADC	4K	3.8K	18 hrs	3.2 hrs	6x
Video ADC	5.8K	5.6K	7 hrs	25 min	15x
Post-Layout					
Sigma-Delta ADC (3 rd)	69K	5K	DNC ¹	29 hrs	Infinite
PLL (1.6GHz, 65nm)	43K	2.9K	3.4 wks	3.2 days	7x
Sigma-Delta ADC (3 rd)	64K	15K	5 days	4.5 hrs	25x
Video ADC	842K	11.3K	8.6 days	16 hrs	13x

Notes:

1. Did not converge.

In the first example AFS reduced a three-week PLL simulation to less than one day, and by doing so made an impractical verification task quite manageable. This is a rather extreme example, but it is by no means unique. The second circuit is a PLL where AFS delivered a 14x speedup, slashing a three-day simulation to less than 5.5 hours. The next three examples are ADCs. AFS reduced the four-day sigma-delta ADC run to about a half day, the pipelined ADC from overnight to 3.2 hours, and the video ADC from seven hours to 25 minutes.

The post-layout 3rd-order sigma-delta ADC had approximately 14x more parasitics than transistors. The traditional SPICE simulator did not converge, but AFS converged and completed transient simulation of the same netlist in just 29 hours with results that were within 1 dB of silicon. Few design teams could afford to devote 3.4 weeks to simulating the post-layout PLL, but most teams would be able to spend the 3.2-day AFS runtime to check their design. The next example is a second sigma-delta ADC in which AFS was

25x faster. The last example in the table is the post-layout version of the pre-layout video ADC. There were 842K total elements and 11.3K transistors in the post-layout netlist: approximately a 75x ratio. Traditional SPICE converged and completed transient simulation in 8.6 days. AFS required only 16 hours. This 13x speedup is comparable to the 15x speedup pre-layout.

This is a small sample of the publicly available AFS results. See the Berkeley Design Automation [Big Analog/RF Verification](#) white paper for a much more comprehensive analysis.

Noise Floor

AFS has a noise floor that is as low or lower than that of traditional SPICE simulators. This gives it the ability to provide higher noise resolution. Figure 9 shows an example of the AFS noise floor advantage on a PLL VCO control signal. In this case the traditional SPICE simulator-induced noise floor was so high that the signal was difficult to discern and the jitter numbers were unusable. The designer was able to lower the noise floor by tightening the traditional SPICE timesteps, but this resulted in unacceptably long simulations. Using the original netlist with its default settings, AFS generated much less simulator numerical noise, providing a sharp signal waveform. It did so 7.4x faster than the traditional SPICE run that produced unacceptable results. This example illustrates the increasing need for even more accuracy than the traditional SPICE defaults provide.

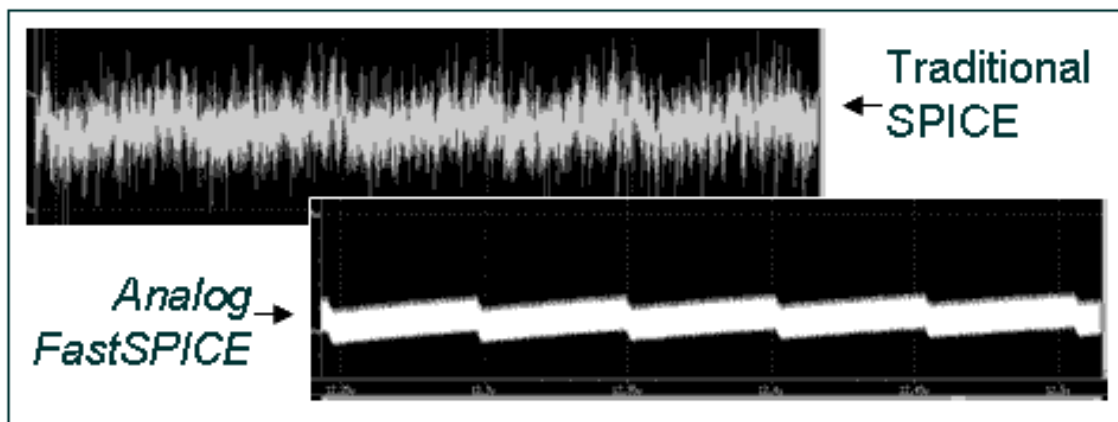


Figure 9. AFS Noise Floor Comparison with Traditional SPICE

7 Noise Analysis Option Transient Noise Analysis

This section describes Berkeley Design Automation Noise Analysis Option (NAO) transient noise analysis and validation of its results. It then presents NAO transient noise analysis results for two sigma-delta ADCs, an integer-N PLL, and a fractional-N PLL. All of these are original production circuits, and in each case the original designer validated the results. It is important to note that NAO provides comprehensive world-class noise analysis including period steady state (PSS) convergence and periodic noise analysis (pnoise) for periodic-driven circuits and oscillator noise analysis (oscnoise/vconoise) for periodic-autonomous circuits.

Capabilities

NAO transient noise analysis provides the following capabilities:

- Noise sources
 - User may select white noise or white noise and flicker noise
 - User may turn off noise for specified blocks
- Noise analysis
 - Generates random noise sources for each noise source at each timestep
 - Uses standard device model noise parameters for white and flicker noise
 - Changes noise intensity with instantaneous bias
- Accuracy, runtime, & capacity
 - True SPICE accuracy down to the SPICE noise floor
 - <2x AFS transient simulation runtime with same timestep count
 - Approximately the same capacity as AFS transient simulation
- Use model
 - Simple 1-2 parameter extension of AFS transient simulation use model
 - Generates standard output waveform formats for any number of nodes
 - Provides sophisticated post-processing environment
 - Supports parallel execution to minimize overall runtime

These capabilities make it practical to run transistor-level noise analysis on ADCs, frac-N PLLs, and int-N PLLs.

Theoretical Validation

NAO transient noise analysis results closely match the theoretical value of kT/C noise. Consider the switch-based sampler circuit in Figure 10. The limit for rms sampled capacitor noise voltage is $\sqrt{kT/C}$.

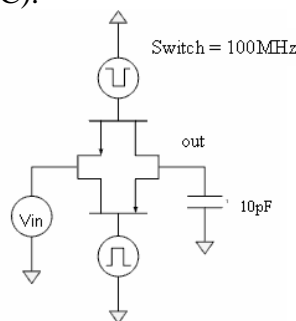


Figure 10. kT/C Sampled Noise Experiment

The simulated standard deviation of the sampled noise voltage will approximate the theoretical value as the number of samples increases. Simulation-based analysis cannot achieve the theoretical value due to nonlinearity effects, charge sharing, and the time-varying nature of the switching MOS devices.

Table 5 shows the NAO transient noise analysis results for this circuit. The error is the difference between the standard deviation from simulation and the theoretical value of $\sqrt{kT/C}$. As the number of samples increases, the simulation results statistically converge to the theoretical value as expected.

Table 5. kT/C Sampled Noise Experiment Results

Samples	Vno(rms)	% Error
1000	20.1e-6	1.5%
2000	19.6e-6	3.9%
4000	19.8e-6	2.6%
8000	20.0e-6	2.0%

Validation with Oscillator Noise Analysis

NAO transient noise analysis results also closely match those of the tool’s oscillator noise analysis. NAO oscillator noise analysis utilizes a proprietary stochastic nonlinear engine that has been silicon-validated by more than 10 leading semiconductor to have ~1 dB relative accuracy and ~2-3 dB absolute accuracy to silicon. [7]

Validating NAO transient noise analysis to NAO oscillator noise analysis consists of comparing the phase noise results for several VCOs. Figure 11 shows a typical overlay of the transient noise results on the oscnoise results. As expected, the results match well.

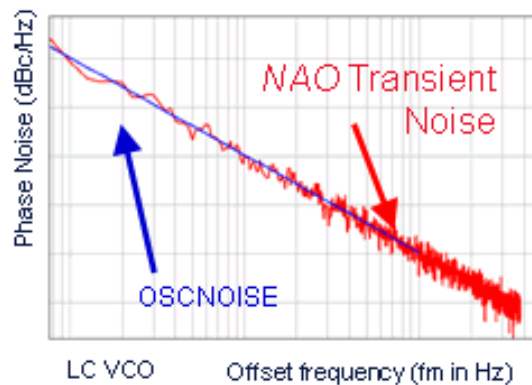


Figure 11. VCO Phase Noise Comparison

ADC Noise Analysis Results

ADCs are complex non-periodic blocks that are often very noise-sensitive. Stringent accuracy requirements and long runtimes make traditional SPICE transient noise analysis impractical. Signal frequency (f_{signal}) and clock frequency (f_{clock}) are the key transient noise analysis circuit parameters, and Signal to Noise and Distortion (SNDR or SINAD) and Effective Number of Bits (ENOB) are the key metrics.

The first sigma-delta ADC example has the following circuit parameters:

- Total elements: 1.4K (1K MOS)
- Signal Frequency: ~20KHz
- Clock Frequency (f_{clock}): ~10MHz

The NAO transient noise analysis run used the following parameters:

- Simulation stop time (t_{stop}): 10 input signal periods= ~500usec
- Noise_{fmax}: 50*f_{clock} = 500MHz
- Noise_{fmin} : 10/t_{stop}= ~ 20KHz

Table 6 summarizes the NAO runtime and key noise metrics for three cases: 1. AFS transient simulation, 2. NAO transient noise analysis with white noise only, and 3. NAO transient noise analysis with white and flicker noise. Figure 12 shows the corresponding power spectral density.

Table 6. NAO Transient Noise Results for Sigma-Delta ADC #1

	Transient Simulation	Transient Noise – White Noise Only	Transient Noise – White & Flicker Noise
AFS/NAO Runtime	~4 hrs	~4.3 hrs	~5 hrs
SNDR	~80 dB	~75 dB	~70 dB
ENOB	~13 bits	~12 bits	~11 bits

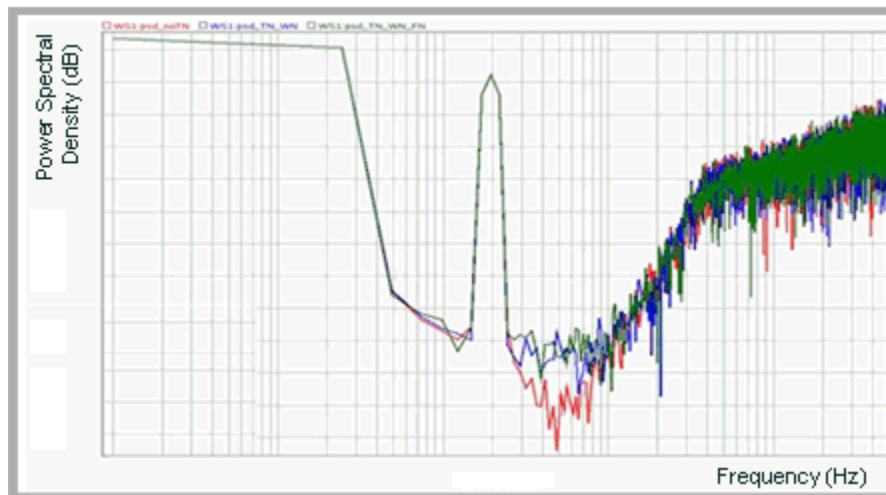


Figure 12. Sigma-Delta #1 ADC Power Spectral Density

The second sigma-delta ADC example has the following circuit parameters:

- Total elements: 6K (1K MOS)
- Signal Frequency: ~60KHz
- Clock Frequency (fclock): ~25MHz

The NAO transient noise analysis run used the following parameters:

- Tstop: 10 input signal per. = ~160us
- Noiseifmax: 50*fclock = ~1.3GHz
- Noiseifmin: 5/tstop = ~31.25KHz

Table 7 summarizes the runtime and key noise metrics for AFS transient simulation and NAO transient noise analysis with white and flicker noise. Figure 13 shows the corresponding power spectral density.

Table 7. NAO Transient Noise Results for Sigma-Delta ADC #2

	Transient Simulation	Transient Noise – White & Flicker Noise
AFS/NAO Runtime	~27 hrs	~50 hrs
SNDR	~76 dB	~75 dB

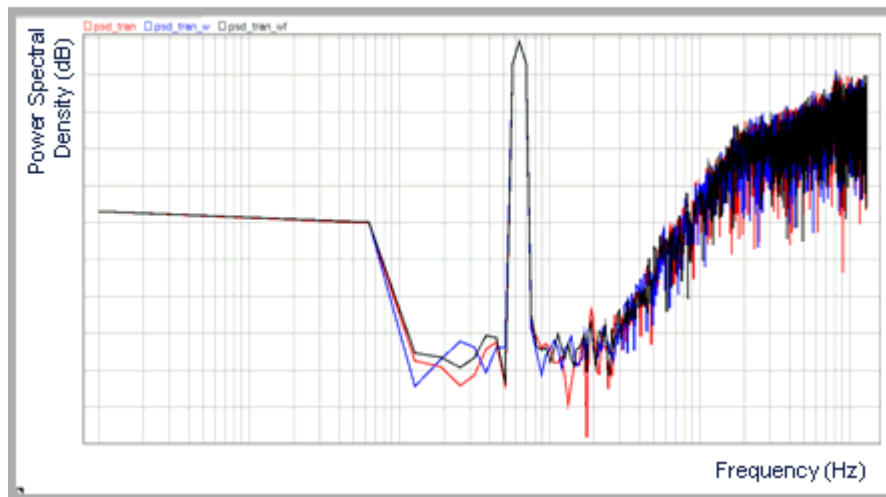


Figure 13. Sigma-Delta #2 ADC Power Spectral Density

Integer-N PLL Noise Analysis Results

It is notoriously difficult to accurately measure phase noise for PLLs because of their topology, complexity, and widely disparate frequencies. VCO frequency (fvco) and minimum offset frequency (minfm) are the key transient noise analysis circuit parameters. Phase noise is the key noise metric.

Figure 14 shows a phase noise profile for a PLL. In this example the phase noise rolls off at 30 dB/decade for low offset frequencies, becomes flat inside the loop bandwidth, rolls off at 20 dB/decade outside the loop bandwidth, and finally assumes a flat noise floor. It may also have a few sets of reference spurs. [8]

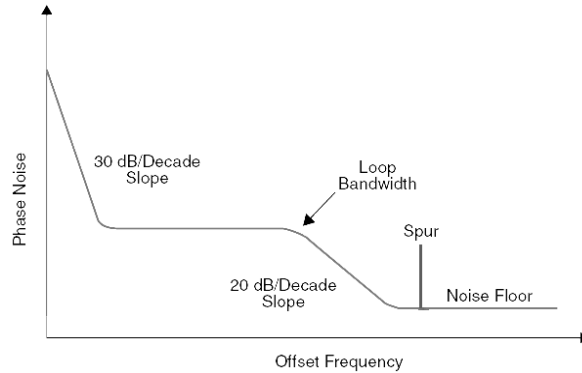


Figure 14. Representative PLL Phase-Noise Profile

The first PLL example is an integer-N architecture with the following circuit parameters:

- Total elements: 2K (2K MOS)
- PLL output frequency: 800 MHz

The NAO transient noise analysis run used the following parameters:

- Tstop: tstab+40/minfm = ~100usec
- Noisefmax: 50*f_{vco} = 40GHz
- Noisefmin: 1/tstop = 10KHz

Figure 15 shows the NAO transient noise analysis results for the integer-N PLL. In this case, the silicon measurements were also available; these measurements are highlighted in the phase noise plot. The transient noise analysis results are in excellent agreement with the phase noise measurements at the specified offset frequencies – within 0.5 dB.

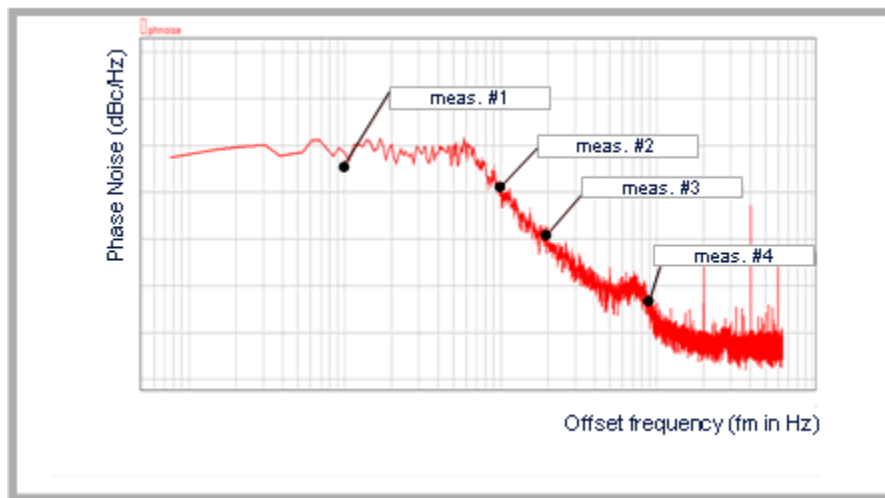


Figure 15. NAO Integer-N PLL Phase Noise Analysis Results

Fractional-N PLL Noise Analysis Results

There has never been a practical method for transistor-level fractional-N PLL phase noise analysis. Periodic noise analysis methods cannot be used due to the non-periodic nature of the sigma-delta modulator. NAO transient noise analysis makes this analysis practical for the first time.

The second PLL example is a fractional-N PLL with the following circuit parameters:

- Total elements: 21K (8K MOS)
- PLL output frequency: 1.5 GHz

The NAO transient noise analysis run used the following parameters:

- Tstop: $t_{stab} + 40 / \text{minfm} = 200\mu\text{s}$
- Noiseifmax: $50 * f_{vco} = 75\text{G}$
- Noiseifmin: $10 / t_{stop} = 50\text{KHz}$

This simulation had also a requirement to verify the phase noise at a low offset frequency. Figure 16 shows the NAO transient noise analysis phase noise plot. Due to the long runtime requirement for the low offset frequency, the analysis consisted of five parallel independent transient noise analysis runs. Each used a tstop adequate for the low offset frequency requirements, a different noiseseed, and a different seed for the sigma-delta modulator. The average of the post-processed results yields the overall result, which appears as the solid black phase noise plot in Figure 16. Again in this case, the transient noise analysis results are in excellent agreement with the phase noise measurements below the PLL loop bandwidth – within 1.5 dB.

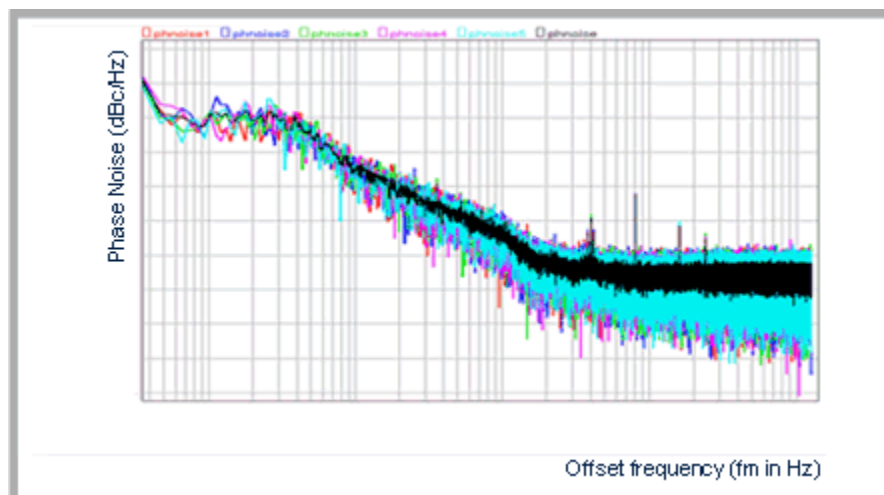


Figure 16. NAO Fractional-N PLL Phase Noise Analysis Results

8 Conclusion

Practical transient noise analysis requires a world-class transient simulation engine with true SPICE accuracy, a very low noise floor, and much higher performance and capacity than traditional SPICE. The Berkeley Design Automation Noise Analysis Option built on the company's Analog FastSPICE circuit simulator uniquely provides all of these capabilities.

This paper has shown how Noise Analysis Option transient noise analysis enables circuit designers to efficiently perform SPICE-accurate noise analysis on complex non-periodic analog/RF blocks. This capability enables designers to measure and optimize noise analysis on complex blocks such as ADCs, frac-N PLLs, and int-N PLLs which would not otherwise have been possible without silicon iterations. The tool's results are in excellent agreement with theoretical, periodic noise analysis, and direct silicon measurements.

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