Streamlining Analog/Mixed-Signal/RF Verification

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Verification methodologies for analog, mixed-signal and radio frequency (AMS/RF) circuits have become complex, inefficient and ineffective. The impact is significant: low designer productivity, long schedules, unnecessary respins, missed specifications, low yield and higher silicon costs — not to mention growing frustration. The key problem is that significant simulator limitations force design teams to constantly tradeoff accuracy, performance, capacity and functionality.

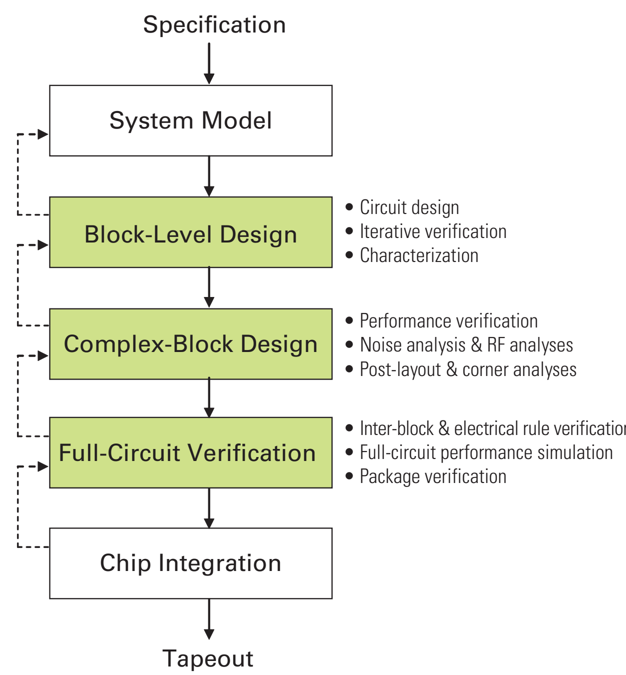
It is time to retool AMS/RF verification. Digital design teams typically retool at every major process node to optimize their flow. By contrast, AMS/RF simulators have stagnated for a decade or longer, leaving design teams to develop increasingly elaborate verification methodologies to overcome increasingly severe tool limitations. As AMS/RF circuits have moved from 0.50-micron to 90-, 65- and even 45-nanometer CMOS processes, their complexity has grown by orders of magnitude. AMS/RF designers must now cope with physical effects that developers of traditional SPICE and RF simulators never anticipated.

Instead of adding yet another verification technique or simulator to work around another tool limitation, leading AMS/RF circuit design teams are completely retooling with a new generation of precision circuit analysis (PCA) tools that provide uncompromising accuracy, 5x to 30x higher performance, 5x to 30x higher capacity and advanced functionality for nanometer physical effects. The resulting precision verification methodologies reduce the AMS/RF design cycle by 30 to 40 percent and enable verification that was previously impractical or impossible.

AMS/RF Verification Methodology Challenges

Verification takes center stage throughout AMS/RF design. Figure 1 illustrates a simplified AMS/RF design methodology and highlights key circuit-level verification tasks. The methodology begins with system designers making architectural decisions based on behavioral models and ends with full-chip integration. This article focuses on common problems in transistor-level AMS/RF verification — the heart of the methodology.

Figure 1. High-Level AMS/RF Verification Methodology



The Need for True SPICE Accuracy

True SPICE accuracy is critical for verifying transistor-level AMS/RF circuits — especially those implemented in nanometer-scale CMOS or operating at GHz frequencies. Inaccuracies of even 1 percent can have a substantial impact on measured specifications and can even produce waveforms with qualitatively incorrect behavior. For example, only 1 percent simulator inaccuracy can add 20dB to the signal-to-noise ratio of a simulated analog-to-digital converter (ADC). The device noise in the same ADC is only 10dB, so the simulation error completely masks the device noise effects. Likewise, even 1 percent inaccuracy makes post-layout simulation, corner analysis, process variation analysis and device noise analysis essentially meaningless.

"True SPICE accuracy" means identical waveforms to industrystandard "golden" SPICE simulators within the SPICE tolerance settings. Default SPICE settings produce a tolerance band of approximately 0.1 percent. This level of accuracy is at least one order of magnitude better than what is practical for behavioral simulation with well-calibrated models, or for digital fastSPICE simulators running with the tightest possible settings.

True SPICE accuracy is even more important for RF simulation. Many RF designers do not realize that traditional RF simulators inherently trade accuracy for performance by limiting the number of sidebands or harmonics they use. Designers can increase the sideband or harmonic count only at the expense of severe penalties in periodic steady state (PSS) convergence capacity; simulator runtime, which may grow quadratically with the number of sidebands or harmonics; and memory consumption.

AMS/RF Block-Level Verification Problems

The first step in transistor-level AMS/RF verification is block-level design, where designers interactively verify schematic-level circuits by using a traditional SPICE simulator. For RF blocks, designers also use a traditional RF simulator. Block-level SPICE simulations generally finish in minutes or tens of minutes. Even these short simulation times can significantly impact designer productivity because of the large number of iterations. For RF blocks, nanometer-scale simulation has become a bottleneck because traditional RF simulators have notoriously poor convergence, even in small blocks, and inherently trade accuracy for performance.

Rigorous characterization is the most serious block-level verification problem. Once a block meets specifications under nominal conditions, designers must characterize it under numerous conditions, including process, voltage and temperature (PVT) corners, and with post-layout parasitics, device noise and, ideally, with process parameter variations. Rigorous characterization can take several days for each block — especially at more advanced process nodes — and require complete re-characterization. Given the explosion in the number of cases at advanced process nodes, traditional SPICE/RF simulators simply do not have enough performance to meet today's competitive design schedules.

AMS/RF Complex Block Verification Problems

Today's most difficult AMS/RF verification challenges begin when integrating complex blocks such as integer-N and fractional-N phase-locked loops (PLLs), high-performance ADCs, memory cores, power converters and receive chains. These circuits exhibit critical emergent functional and performance characteristics that designers cannot analyze at the block level.

Complex blocks often contain tens of thousands of elements. These blocks can be highly non-linear, sensitive to device noise and parasitics, and subject other nanometer physical effects. Even minor simulation inaccuracies can produce results that are not only quantitatively inaccurate, but actually functionally incorrect. In fact, it may be desirable or necessary to simulate complex blocks with tighter-than-the-default SPICE tolerances, for example, to get an acceptable simulation result for the circuit's dynamic range. Doing so can cause traditional SPICE convergence failure or impose serious runtime penalties.

Designers would like to characterize complex blocks as thoroughly as they would characterize block-level circuits. Such characterization should include pre-layout transient simulation, post-layout transient simulation, variation analysis (corners analysis and/or Monte Carlo), random and deterministic noise analysis, and periodic analysis for RF circuits. All these analyses require true SPICE accuracy, yet even a single pre-layout simulation with traditional SPICE may require days or weeks, which is not practical in the required time-to-market window. Without a practical way to sufficiently characterize these circuits, designers must add sufficient margin or accept increased risk.

Design teams that use traditional SPICE and RF tools for complex blocks must make difficult decisions — all of which sacrifice accuracy. They can take shortcuts with traditional SPICE/RF simulators (e.g., by simplifying the circuit or by combining block-level analysis), substitute behavioral models for transistor-level circuitry or use digital fastSPICE simulators. All these techniques sacrifice enough accuracy to yield highly questionable results. To mitigate the added risk, designers must add block-level design margin. As a result, these techniques are potentially very expensive in terms of circuit performance specifications, power consumption and silicon cost. They also require a more complex methodology that saps valuable designer productivity and lengthens the project.

Full-Circuit Verification Problems

Full-circuit integration is the stage at which all transistor-level circuitry and embedded digital logic is integrated. Today's top-level, pre-layout circuits often contain 100,000 to 1 million elements. Parasitics can easily increase the size by 10x to 20x. At this stage in the design flow, it is important to verify the inter-block connectivity and interactions. Validating connectivity minimally requires simulation of the direct current (DC) operating point for the full circuit. Traditional SPICE does not have sufficient capacity to do so, and digital fastSPICE tools do not generate electrically valid operating points. Design teams work around these limitations by generating DC operating points for combinations of blocks or relying on relaxed accuracy "functional verification" to identify problems. Both approaches are time-consuming and may miss connectivity problems.

Verifying inter-block interfaces requires electrical rule checking, which is becoming increasingly complicated in circuits with multiple modes for various configurations, standards and power settings. Today, this often involves manually monitoring key waveforms, using circuit-level assertions and validating full-circuit outputs during interface corner-case tests. Such tests are accurate and reliable only with true SPICE-accurate simulation, but again SPICE simulators rarely have sufficient capacity or performance for such verification.

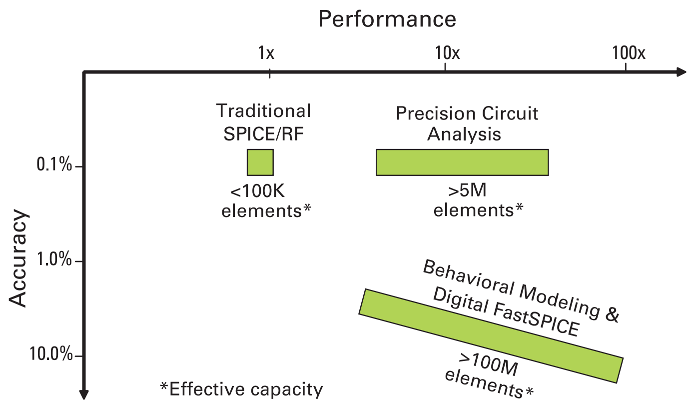
Full-circuit verification is the only opportunity to verify key IC performance specifications prior to measuring first silicon. Again, this requires true SPICE-accurate simulation, which is unthinkable with traditional tools, even when the embedded digital logic is co-simulated with a digital hardware description language (HDL) simulator. At this point, it is also important to verify high-frequency or highly sensitive interface circuits while including the package effects. Since this requires performance simulation with package models (including s-parameters and inductors), which is impractical or impossible with today's simulators, designers must create simplified models or margin the circuit.

Streamlining Methodologies with PCA Tools

Design teams using traditional AMS/RF verification tools must continuously make tradeoffs throughout their verification methodology due to tool accuracy, performance, capacity and functional limitations. While abstraction is useful during system design, once the design reaches the transistor level, it is easiest, fastest and safest to use the transistor-level circuit thereafter without shortcuts that sacrifice accuracy. Streamlining AMS/RF verification requires tools that provide true SPICE accuracy with much higher performance, much higher capacity and the full functionality required to address critical nanometer CMOS verification challenges such as post-layout and device noise analyses.

A new generation of PCA tools provides a foundation for streamlined verification, including delivering true SPICE accuracy 5x to 30x faster and with 5x to 30x higher capacity than traditional circuit and RF simulation tools — all with full functionality. As shown in Figure 2, these tools combine the accuracy of traditional SPICE/RF simulators with the performance and capacity that behavioral modeling and digital fastSPICE can only deliver along with unacceptable accuracy.

Figure 2. PCA Tool Accuracy, Performance and Capacity



Using PCA tools, designers can focus on adding value during design rather than on making complex verification tradeoffs. Simulations that always provide true SPICE accuracy require no tradeoffs, no special tool setup or tuning, and no detailed checks of the verification results to try to determine if they are “accurate enough.” With 5x to 30x higher performance, PCA tools slash runtimes from hours to minutes, days to hours, and weeks to days. This enables rapid turnaround times, less designer down time and less designer context switching. The result is a proven 30 to 40 percent decrease in overall design cycle time versus methodologies based on last-generation tools.

Block-Level Verification Results

At the block level, PCA tools enable higher productivity through faster design iterations, especially for more challenging blocks. Increased performance makes it possible to rigorously characterize blocks through extensive post-layout, device noise, PVT and process parameter analyses. In addition, PCA tools have capabilities, such as robust RF analysis, that never sacrifice accuracy for performance, enabling RF designers to optimize the silicon implementation. PCA tools enable:

- >5x faster iterations for complex blocks.
- Rigorous block characterization with parasitics, device noise and variations.
- Robust RF analyses with true SPICE accuracy on blocks with >100,000 elements.

Complex Block Verification Results

Combining true SPICE accuracy, much higher performance and new features, PCA tools enable verification of critical emergent properties even on highly complex and sensitive circuits. One example is closed-loop, transistor-level noise analysis (including device thermal and flicker device noise) for integer-N and fractional-N PLLs. Applications such as these are literally impossible without PCA tools. Another example is ADC verification, including the effects of device noise, with a simplified transient noise analysis rather than a complex block-level approach that yields only approximate results. Example applications include:

- PLL closed-loop, transistor-level noise analysis that includes device noise.
- ADC signal-to-noise-and-distortion ratio that includes device noise.
- Transistor-level memory characterization that includes parasitics.

Full-Circuit Verification Results

Capacity becomes essential for full-circuit verification. PCA tools robustly generate DC operating points and perform transient analysis on multi-million element circuits. Unlike behavioral or digital fastSPICE approaches, all waveforms have true SPICE accuracy, so design teams get realistic full-circuit performance waveforms and circuit metrics every run. PCA tools support package models and integrated co-simulation with digital logic and behavioral Verilog-A, enabling full-circuit verification that was previously impossible. Example applications include:

- DC operating point simulations for circuits with over five million elements.
- Full-transceiver, transistor-level inter-block interface validation.
- High-speed interface performance simulation with parasitics and packaging.

Summary

Design teams developing nanometer-scale AMS/RF circuits have been forced to create complex, time-consuming verification methodologies due to fundamental limitations in traditional SPICE and RF simulation tools. Such approaches have become extremely burdensome, introducing substantial risk and keeping designers from what they do best — adding value through architectural tradeoffs, superior circuit design and hand-crafted implementation.

A new generation of PCA tools makes no comprises. PCA tools deliver true SPICE accuracy with full functionality 5x to 30x faster and with 5x to 30x higher capacity than traditional circuit and RF simulation tools. These capabilities enable a systematic 30 to 40 percent reduction in the overall AMS/RF design cycle, and the ability to perform verification tasks that were otherwise impractical or impossible. A growing number of companies, from the largest semiconductor suppliers to leading-edge start-ups, have already used PCA tools to verify thousands of circuits in record time, using less effort and with unprecedented confidence. ■

About the Author

Paul Estrada is chief operating officer at Berkeley Design Automation in Santa Clara, California. His prior experience includes executive positions at Cadence, 0-In Design Automation and Synopsys. He has engineering degrees with honors from Stanford University and University of Illinois, and holds three patents. You can reach Paul Estrada at pi@berkeley-da.com.